IN THE CLAIMS

Please rewrite claims 1, 9, 10, 12 and 13 as follows:

1. (Currently Amended): An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit having protected circuitry, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) having an anode coupled to the protected circuitry and a cathode coupled to ground, said cathode having at least one first high-doped region;

at least one trigger-tap, disposed proximate to the at least one high-doped region; and

an external on-chip triggering device coupled to the trigger-tap and the protected circuitry.

2. (Previously Amended): The ESD protection circuit of claim 1, further comprising a lateral shunt resistor coupled between the cathode and the external triggering device.

3. (Original): The ESD protection circuit of claim 1, wherein the SCR comprises a first bipolar transistor T1 and a second bipolar transistor T2; said first bipolar transistor having the at least one first high doped region serving as an emitter and forming the cathode, a first low doped region coextensively forming a base of the first bipolar transistor T1 and a collector of the second bipolar transistor T2, a second low doped region coextensively forming a base of the second bipolar transistor T2 and a collector of the first bipolar transistor T1, and a second high doped region serving as an emitter of the second bipolar transistor T2 and forming the anode.

4. (Previously Amended): The ESD protection circuit of claim 3, wherein a surface area between the respective first and second high-doped regions of the first and second bipolar transistors are blocked from shallow trench isolation.

5. (Original): The ESD protection circuit of claim 3, wherein the bases of the first and second transistors have base widths less than 4.0 microns.

6. (Original): The ESD protection circuit of claim 5, wherein the bases of the first and second transistors have base widths in a range of 0.6 to 0.8 microns.

7. (Original): The ESD protection circuit of claim 3, wherein the at least one first high doped region is a N+ type material, the first low doped region is a P-type material, the second low doped region is a N-type material, and the second high doped region is a P+ type material.

8. (Original): The ESD protection circuit of claim 7, wherein the triggering device is a MOSFET transistor selected from the transistor group consisting of a NMOS, a NMOS provided with drain-bulk-gate coupling, a NMOS in an isolated P-well, at least two cascoded NMOS transistors, and a ballasted NMOS.

9. (Currently Amended): The ESD protection circuit of claim 8, wherein [the]a source and a drain of the MOSFET transistor are respectively coupled to the trigger-tap and to the protected circuitry.

10. (Currently Amended): The ESD protection circuit of claim 9, wherein [the]a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the NMOS, the NMOS in an isolated P-well, the at least two cascoded NMOS transistors, and the ballasted NMOS.

11. (Original): The ESD protection circuit of claim 7, wherein the triggering device is a MOSFET transistor selected from the transistor group consisting of a PMOS, a PMOS provided with drain-bulk-gate coupling, a PMOS in an isolated N-well, at least two cascoded PMOS transistors, and a ballasted PMOS.

12. (Currently Amended): The ESD protection circuit of claim 11, wherein [the]a drain and a source of the MOSFET transistor are respectively coupled to the trigger-tap and the protected circuitry.

13. (Currently Amended): The ESD protection circuit of claim 12, wherein [the] a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the PMOS, the PMOS in an isolated N-well, the at least two cascoded PMOS transistors, and the ballasted PMOS.

14. (Original): The ESD protection circuit of claim 3, wherein a surface area between the respective first and second high-doped regions of the first and second bipolar transistors are shallow trench isolated.

15. (Previously Amended): An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:

a SCR further comprising:

a substrate;

a N-well and an adjacent P-well formed in said substrate and defining a junction therebetween;

at least one N+ doped region in said P-well and coupled to ground;

a P+ doped region in said N-well and coupled to a pad of said protected circuitry;

at least one P+ doped trigger tap disposed proximate to at least one N+ doped region in said P-well; and

an external on-chip triggering device coupled to the SCR, wherein one terminal is coupled to the pad and a second terminal is coupled to the trigger tap.

16. (Original): The ESD protection circuit of claim 15, wherein the second terminal is further coupled to ground via a shunt resistor.

17. (Previously Amended): The ESD protection circuit of claim 15, wherein a surface area between the at least one N+ doped region and the P+ doped region is shallow trench isolation blocked.

18. (Original): The ESD protection circuit of claim 15, wherein respective base widths between the P+ doped region and the junction, and between the at least one N+ doped region and the junction are less than 4.0 microns.

19. (Original): The ESD protection device of claim 15, wherein a P-well-tie is coupled to the P-well and grounded.

20. (Original): The ESD protection circuit of claim 15, wherein the triggering device is a MOSFET transistor selected from the transistor group consisting of a NMOS, a NMOS provided with drain-bulk-gate coupling, a NMOS in an isolated P-well, at least two cascoded NMOS transistors, and a ballasted NMOS.

21. (Currently Amended): The ESD protection circuit of claim 20, wherein [the]a source and a drain of the MOSFET transistor are respectively coupled to the trigger-tap and the pad.

22. (Currently Amended): The ESD protection circuit of claim 21, wherein [the]a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the NMOS, the NMOS in an isolated P-well, the at least two cascoded NMOS transistors, and the ballasted NMOS.

23. (Original): The ESD protection circuit of claim 15, wherein a surface area over a non high-doped region and between the P+ doped region and the at least one N+ doped region is fully shallow trench isolated.

24. (Previously Amended): An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:

a SCR further comprising:

a substrate;

a P-well and an adjacent N-well formed in said substrate and defining a junction therebetween;

at least one P+ doped region dispersed in said N-well;

a N+ doped region dispersed in said P-well and coupled to ground;

at least one N+ doped trigger tap disposed proximate and between the at least one P+ doped region in said N-well; and

a PMOS transistor triggering device coupled to the SCR, wherein a drain is coupled to ground and a source is coupled to the trigger tap; the at least one P+ doped region is further coupled to a pad; the source is further coupled to the pad via a shunt resistor; and the pad is further coupled to said protected circuitry.

25. (Original): The ESD protection circuit of claim 24, wherein a surface area over a non-high-doped region and between the at least one P+ doped region and the N+ doped region is shallow trench isolation blocked.

26. (Original): The ESD protection device of claim 24, wherein a N-well tie is coupled to the N-well and coupled to the pad.

27. (Original): The ESD protection circuit of claim 24, wherein the triggering device is a PMOS transistor selected from the transistor group consisting of a PMOS, a PMOS provided with drain-bulk-gate coupling, a PMOS in an isolated N-well, at least two cascoded PMOS transistors, and a ballasted PMOS.

28. (Currently Amended): The ESD protection circuit of claim 27, wherein [the]a source and a drain of the MOSFET transistor are respectively coupled to the at least one trigger-tap and ground.

29. (Currently Amended): The ESD protection circuit of claim 28, wherein [the]a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the PMOS, the PMOS in an isolated N-well, the at least two cascoded PMOS transistors, and the ballasted PMOS.

30. (Original): The ESD protection circuit of claim 24, wherein respective base widths between the N+ doped region and the junction, and between the at least one P+ doped region and the junction are less than 4.0 microns.

31. (Original): The ESD protection circuit of claim 24, wherein a surface area over a non high-doped region and between the N+ doped region and the at least one P+ doped region is fully shallow trench isolated.